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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PRITCHETT, JOSHUA L	
ART UNIT	PAPER NUMBER
2872	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No. 09/872,306	Applicant(s) CARR ET AL.	
	Examiner Joshua L Pritchett	Art Unit 2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action is in response to Amendment B filed July 7, 2003. Claims 1, 4, 7 and 12 have been amended as requested by the applicant.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 6, 11, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani (US 6,433,411) in view of Ikuina (US 5,952,712) and Higuchi (JP 09261975).

Regarding claims 1 and 13, Degani teaches an array (col. 3 lines 15-16) of electrostatically activated members (col. 3 lines 7-8) formed on a layer comprising silicon (col. 3 line 30; Fig. 2 (32)). Degani further teaches a substrate comprising a ceramic material (col. 5 lines 15-16; Fig. 3 (52)). Degani further teaches contact pins passing through holes in the ceramic substrate (col. 5 lines 20-23; Fig. 3 (56)). It is not completely clear whether these contact pins serve as conductors; therefore the examiner will assume the pins are not conductors.

Degani lacks conductors attached to the ceramic substrate. Degani further lacks conductors in via holes formed in the substrate to operate the array of members and the conductors positioned separate from the silicon layer. Degani further lacks conductors formed on a major surface of the substrate. Ikuina teaches the use of conductors (17) on a ceramic substrate (12) with via holes (15) in the substrate and the substrate connected to a silicon layer (11). It is not clear if the conductors (17) of Ikuina are inside via holes (15) therefore the examiner will assume the conductors are not passing through the via holes. Ikuina teaches the conductors being positioned separate from the silicon layer (Fig. 1). Higuchi teaches the use of via holes (3) through a substrate (1) to selectively operate an array of members. Higuchi teaches that the substrate with through holes acts as an electrostatic actuator (translation page 1). Higuchi further teaches conductors (B, Fig. 7) formed on the major surface of the substrate (1, Fig. 7). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the through hole electrostatic actuator and the conductors on the major surface of the substrate taught by Higuchi in the Degani invention for the purpose of creating a more electrically isolated environment around the micromirrors therefore allowing the tilting to be more precise.

Regarding claims 2 and 14, Degani teaches a device where the members are rotatable mirrors (col. 2 line 66; Fig. 1 (11a-i)).

Regarding claims 4 and 17, Degani teaches the array element separated from the substrate by a spacer layer (col. 5 lines 29-32). Degani teaches the member floats on the interconnect substrate therefore the spacer layer between the substrate and the member is air.

Regarding claim 6, Degani teaches the mirrors are adapted to rate about at least two axes (col. 3 lines 5-6; Fig. 1 (15-18)).

Regarding claim 11, Degani teaches the conductors positioned to operate a member comprise an array of at least four conductors (col. 3 lines 11-12; Fig. 1 (15-18). Degani lacks specific reference to the conductors in via holes. Higuchi teaches the use of conductors in via holes (translation page 1). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the conductors of Degani in via holes as taught by Higuchi for the purpose of achieving greater electrical isolation of the members.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi as applied to claim 2 above, and further in view of Lin "Free-Space Micromachined Optical Switches for Optical Networking".

Degani suggest the possibility of creating larger arrays than the 3x3 array disclosed, but does not explicitly disclose larger arrays (col. 3 lines 11-12). Degani in combination with Ikuina and Higuchi teaches the invention as claimed but lack the claimed dimension of the array. Lin teaches that the array can be extended to include an array of at least 8x10 (page 8 col. 2). Lin discloses arrays of various sizes that exceed 8x10. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an array of at least 8x10 as taught by Lin in combination with the invention of Degani and Higuchi for the purpose of storing more data on a single chip.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi as applied to claim1 above, and further in view of Engleberth (US 6,393,187).

Degani in combination with Ikuina and Higuchi teaches the invention as claimed but lack reference to a metal layer dispersed on the silicon layer. Engleberth teaches an optical array device comprising a layer of metal on a major surface of a silicon layer (col. 3 lines 23-26). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to deposit a metal layer as taught by Engleberth on the silicon layer of Degani and Higuchi for the purpose of filling exposed cavities in the silicon layer.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi as applied to claim 1 above, and further in view of Imanaka "Thin Film Metallization for Aluminum Nitride".

Regarding claim 7, Degani teaches the metallization of aluminum to provide electrical interconnection between the substrate and MEMS device (col. 3 lines 59-64). Degani, Ikuina and Higuchi lack reference to the use of aluminum nitride as the ceramic used as the substrate. Imanaka teaches the use of aluminum nitride substrates in microelectronics (page 1 para. 3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use aluminum nitride as the ceramic substrate in the Degani invention for the purpose of creating a device that can operate at high temperatures.

Regarding claim 9, Degani in combination with Ikuina and Higuchi teaches the invention as claimed but lack reference to the roughness of the substrate. Imanaka teaches the roughness of the substrate to be less than one micron (page 1 para. 3). Imanaka discloses a roughness of less than 0.3 microns. It would have been obvious to a person of ordinary skill in the art at the

time the invention was made to create the Degani substrate with the roughness taught by Imanaka for the purpose of creating a precise signal from the MEMS device.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi as applied to claim1 above, and further in view of Lin.

Degani in combination with Ikuina and Higuchi teaches the invention as claimed but lack reference to a substrate flatness of less then 10 microns. Lin teaches a substrate flatness of less than 10 microns (page 5 col. 2). Lin discloses a flatness of 5000 Angstroms, which is equivalent to 0.5 microns. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have the substrate flatness of Lin on the Degani and Higuchi device for the purpose of producing precise signal.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi as applied to claim 1 above, and further in view of Fjelstad (US 6,329,607) and Farrar (US 6,284,656).

Degani in combination with Ikuina and Higuchi teaches the invention as claimed but lack reference to the size and spacing of the conductors. Fjelstad teaches a conductor of less than 2 microns in width (col. 5 lines 3-4). Fjelstad discloses a conductor having a line width of least than 10 microns. Farrar teaches conductors having spacing of less than 2 microns (col. 5 lines 46-48). Farrar discloses submicron spacing of conductors. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the conductor size of

Fjelstad and the conductor spacing of Farrar in the invention of Degani and Higuchi for the purpose of creating a smaller chip capable of performing the same tasks as a larger chip.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi and Lin and Imanaka.

Degani teaches an array of mirrors (col. 2 line 66) rotatable about at least two axes (col. 3 lines 5-6) formed in a layer comprising silicon (col. 3 line 29). Degani further teaches the array element separated from the substrate by a spacer layer (col. 5 lines 29-32). Degani discloses the member floats on the interconnect substrate therefore the spacer layer between the substrate and the member is air. Degani teaches a substrate comprising a ceramic material (col. 5 lines 15-16; Fig. 3 (52)). Degani lacks reference to conductors formed directly on the ceramic substrate. Degani further lacks reference to the claimed size of the array. Degani further lacks reference to the use of aluminum nitride as the ceramic material used in the substrate. Degani further lacks reference to the flatness and roughness of the substrate. Degani further lacks specific reference to conductors in via holes and conductors positioned separate from the silicon layer. Ikuina teaches the use of conductors (17) disposed on a ceramic substrate (12) and the ceramic substrate comprising through holes (15). Ikuina teaches the conductors being positioned separate from the silicon layer (Fig. 1). Lin teaches that the array can be extended to include an array of at least 8x10 (page 8 col. 2). Lin discloses arrays of various sizes that exceed 8x10. Lin teaches a substrate flatness of less than 10 microns (page 5 col. 2). Lin discloses a flatness of 5000 Angstroms, which is equivalent to 0.5 microns. Imanaka teaches the roughness of the substrate to be less than one micron (page 1 para. 3). Imanaka discloses a roughness of less than 0.3

microns. Imanaka teaches the use of aluminum nitride substrates in microelectronics (page 1 para. 3). Higuchi teaches the use of via holes (3) through a substrate (1) to selectively operate an array of members. Higuchi teaches that the substrate with through holes acts as an electrostatic actuator (translation page 1). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to equip the Degani substrate with the ceramic material taught by Imanaka and to have the substrate have the roughness and flatness taught by Imanaka and Lin respectively for the purpose of creating a microelectronic device that can withstand high temperatures and have precise signaling. It would also have been obvious to increase the size of Degani to an array of at least 8x10 as taught by Lin for the purpose of processing more information on a single chip. It would further have been obvious to a person of ordinary skill in the art at the time the invention was made to equip the Degani substrate with via holes and to place the conductors in the via holes for the purpose of achieve electrical isolation of the members.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi as applied to claim 13 above, and further in view of Aksyuk (US 5,995,688).

Degani in combination with Ikuina and Higuchi teaches the invention as claimed but lacks reference to the bonding method of the silicon layer. Aksyuk teaches the silicon layer mounted through either an epoxy or solder bond (col. 7 lines 34-35). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the bonding

techniques of Aksyuk in the invention of Degani and Higuchi for the purpose of creating a strong and durable bond on the silicon layer.

Response to Arguments

Applicant's arguments filed July 7, 2003 have been fully considered but they are not persuasive.

On pages 5-6 of Amendment B, applicant argues that Ikuina lacks a ceramic substrate for all the electrical connections. Claims 1 and 13 state "conductors formed on a major surface" of ceramic substrate and claim 1 further states, "conductors on the silicon layer is not required." Claims 12 states, "the conductors remain separate from said silicon layer." These limitations with the broadest reasonable interpretation of one of ordinary skill in the art do not mean that all conductors must be on the ceramic substrate as argued by the applicant. "The conductors" referred to are the ones on the ceramic substrate and do not preclude any conductors on the silicon layer just that the conductors on the ceramic layer be separate from the silicon layer. The examiner therefore believes the claims still read on the prior art of record.

On pages 6-8 of Amendment B, applicant argues that all the dependent claims of the application should be allowable because the independent claims are allowable. As stated above the examiner feels that the independent claims are not allowable and therefore the dependent claims are also rejected.

On page 9 of Amendment B, applicant argues that Aksyuk lacks the silicon layer bonded to a ceramic layer. Aksyuk was used in the rejection to teach the silicon layer can be bonded

using the claimed method. Ikuina was used in the rejection to teach a silicon layer bonded with a ceramic layer. The combination of teachings discloses the claimed invention as is motivated as discussed in the rejection above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua L Pritchett whose telephone number is 703-305-7917. The examiner can normally be reached on Monday - Friday 7:00 - 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew A Dunn can be reached on 703-305-0024. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JLP

DREW DUNN
SUPERVISORY PATENT EXAMINER